

**Syllabus:**

CS 5390: Advanced Systems and Architecture Topics  
Summer 2014

**Instructors:**

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**Class time and location:**

TR 1:30-3:20pm, CCSB 1.0510

**Course website:** <http://svmoore.pbworks.com>

**Course description:**

This course focuses on advanced system-level architecture for systems ranging from mobile devices to warehouse-scale datacenters. It covers topics such as cache hierarchies, memory systems, non-volatile storage, virtualization, power management, and hardware-software co-design. Non-traditional and emerging architectures such as reconfigurable systems, logic-in-memory, and network computers are also of interest. Coursework will consist of reading and discussions of survey and research papers, as well as programming projects. The programming projects will provide an introduction to performance analysis and optimization techniques for computer systems. Objectives of the course are to understand organization of computer systems so as to be able to:

- analyze and evaluate computer systems with respect to performance, power consumption, and reliability
- discuss design tradeoffs in meeting system requirements
- evaluate emerging architectures

The course is intended for graduate students specializing in the field of computer systems who wish to understand and make efficient use of modern computer systems of various scales.

**Tentative reading list:**

[Daniel J. Sorin](#), Mark D. Hill, [David A. Wood](#): A Primer on Memory Consistency and Cache Coherence. [Synthesis Lectures on Computer Architecture](#), Morgan & Claypool Publishers 2011

[Milo M. K. Martin](#), Mark D. Hill, [Daniel J. Sorin](#): Why on-chip cache coherence is here to stay. [Commun. ACM](#) 55(7): 78-89 (2012)

[Arkaprava Basu](#), Mark D. Hill, [Michael M. Swift](#): Reducing memory reference energy with opportunistic virtual caching. [ISCA 2012](#): 297-308

[Undersubscribed Threading for High-Performance and Energy-Efficient Many-Core Execution](#), Wim Heirman, Trevor Carlson, Kenzo Van Craeynest, Ibrahim Hur, **Aamer Jaleel**, Lieven Eeckhout. *In International Conference on High Performance Computer Architecture (HPCA)*, Orlando, Florida, February 2014.

James E. Smith, Ravi Nair, "The Architecture of Virtual Machines," *IEEE Computer*, vol. 38, no. 5, pp. 32-38, May 2005, doi:10.1109/MC.2005.173

Qiuling Zhu, Tobias Graf, H. Ekin Sumbul, Larry Pileggi, Franz Franchetti, "Accelerating Sparse Matrix-Matrix Multiplication with 3D-Stacked Logic-in-Memory Hardware", *HPEC'13*, Waltham, MA, Sept. 2013.

Exploiting Free Silicon for Energy-Efficient Computing Directly in NAND Flash-based Solid-State Storage Systems Peng Li, University of Minnesota; Kevin Gomez, Seagate Technology; David Lilja, University of Minnesota, *HPEC'13*, Waltham, MA, Sept. 2013

### [\*\*A High Performance and Memory Efficient LU Decomposer on FPGAs\*\*](#)

[Guiming Wu](#), [Yong Dou](#), [Junqing Sun](#), Gregory D. Peterson

Journal: [IEEE Transactions on Computers - TC](#) , vol. 61, no. 3, pp. 366-378, 2012

Samuel Williams, Andrew Waterman, and David Patterson. 2009. Roofline: an insightful visual performance model for multicore architectures. *Commun. ACM* 52, 4 (April 2009), 65-76. DOI=10.1145/1498765.1498785 <http://doi.acm.org/10.1145/1498765.1498785>

Jee Whan Choi and Richard Vuduc. A roofline model of energy. Technical Report GT-CSE-12-01, Georgia Institute of Technology, School of Computational Science and Engineering, Atlanta, GA, USA, December 2012. <https://smartech.gatech.edu/xmlui/handle/1853/45737>.

Bruno da Silva, An Braeken, Erik H. D'Hollander, and Abdellah Touhafi, "Performance Modeling for FPGAs: Extending the Roofline Model with High-Level Synthesis Tools," *International Journal of Reconfigurable Computing*, vol. 2013, Article ID 428078, 10 pages, 2013. doi:10.1155/2013/428078

Kenneth Czechowski and Richard Vuduc. A theoretical framework for algorithm-architecture co-design. In *Proc. IEEE Int'l. Parallel and Distributed Processing Symp. (IPDPS)*, Boston, MA, USA, May 2013. doi:10.1109/IPDPS.2013.99.