EE 4342 --- Digital Systems Design II

Spring 2020

Instructor: Dr. P. Nava
Office: A-315
Office Hours: 11:00 – 12:00 Monday
2:00 – 2:50 Tuesday and Thursday
Other times by appointment
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Course Description: Design techniques for complex digital systems, with emphasis on computer hardware design and computer-aided techniques, including hardware description languages and hardware simulation packages. Algorithmic State Machine design is stressed for small systems. Emphasis on problem definition, design, and verification.

Prerequisite: EE 3376 with a grade of “C” or better. Prerequisite by Topic:
(1) combinational and sequential digital design techniques
(2) basic microprocessor architecture
(3) assembly language programming
(4) High-Level language programming

Corequisite: EE 4142 LAB: Design and verification of digital systems using simulation. Laboratory implementation using standard, integrated circuits and programmable logic devices.

Students completing EE 4342 will be able to:
1. Apply different design methods for digital circuitry from problem statement to physical implementation.
2. Use good design techniques, especially top-down design such as the ASM method.
3. Recognize and apply typical hardware constructs for processing units.
4. Recognize and apply typical hardware constructs for control units: hardwired and microprogrammed.
5. Write microcode using standard microcoding techniques.
6. Use processor peripheral support chips, such as MMUs, interrupt chips, etc.
7. Use computer aided tools to simulate and verify designs.
8. Find information on specific chips, and how to obtain application notes.
Topics Covered:
1. Review of combinational and sequential digital design techniques, HDL representation, memory components and PLDs
2. Algorithmic state machine design procedure
3. Datapath (CPU) operations and design; design of a control word
4. Sequencing and Control: hardwired and microprogrammed
5. Instruction set architecture
6. I/O, communication and memory systems (if time allows)

Course Grading:

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
<th>Scale</th>
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<tbody>
<tr>
<td>Homework and Quizzes</td>
<td>20%</td>
<td>90% – 100% → A</td>
</tr>
<tr>
<td>Exams (4 equally weighted).....</td>
<td>75%</td>
<td>80% – 89% → B</td>
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<tr>
<td>Instructor assessment ..........</td>
<td>5%</td>
<td>70% – 79% → C</td>
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<td>60% – 69% → D</td>
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<td>0% – 59% → F</td>
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Scale:

- 90% – 100% → A
- 80% – 89% → B
- 70% – 79% → C
- 60% – 69% → D
- 0% – 59% → F

Academic Integrity:

As an entity of The University of Texas at El Paso, the Department of Electrical and Computer Engineering is committed to the development of its students and to the promotion of personal integrity and self-responsibility. The assumption that a student’s work is a fair representation of the student’s ability to perform forms the basis for departmental and institutional quality. All students within the Department are expected to observe appropriate standards of conduct. Acts of scholastic dishonesty such as cheating, plagiarism, collusion, the submission for credit of any work or materials that are attributable in the whole or in part to another person, taking an examination for another person, any act designed to give unfair advantage to a student, or the attempt to commit such acts will not be tolerated. Any case involving academic dishonesty will be referred to the Office of Student Conduct and Conflict Resolution. The Dean will assign a Student Judicial Affairs Coordinator who will investigate the charge and alert the student as to its disposition. Consequences of academic dishonesty may be as severe as dismissal from the University. See the details of Academic Integrity and formal definitions of Scholastic Dishonesty at [http://sa.utep.edu/osccr/academic-integrity](http://sa.utep.edu/osccr/academic-integrity) for more information.

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