Instructor Information: included in student handout

Course Description: Implementation and testing of combinational and sequential digital systems.

Text: none

Required Materials:
1) Engineering notebook (composition book with grid pages)
2) USB Removable Flash Drive
3) ECE Vectra Lab Student Computer Account (Acquired at Room E319 B)

Prerequisite: EE 1305 and EE 1105, each with a grade of “C” or better; or CS 1301 and CS 1101, each with a grade of “C” or better; or CS 1401 with a grade of “C” or better.

Co-requisite: EE 2369 (Digital Systems Design I). There are hardware projects and software simulation projects, performed in this lab, that are associated with this class. The student is responsible for completing the labs, and meeting with the Teaching Assistant at the formally scheduled time assigned to the section in which the student registered. Please note that the lab is 1 credit hour, and the grade for that lab is calculated separately from the grade in this class.

Course Outcomes:
At the end of this course students will be able to:
- Utilize the standard design sequence outlined below to create Digital Logic Systems;
- Use the Xilinx ISE development environment to implement designs;
- Implement Digital Logic Systems in various forms;
- Use the Xilinx Spartan 3 (or similar) FPGA Chipset as target hardware for implementation; and
- Design via Verilog (HDL) or schematic capture modules found in the development platform.

Design Sequence:
1) Design Creation (schematic capture or HDL)
2) Synthesis (create design into a gate-level netlist)
3) Constraints (specify timing constraints and I/O assignment)
4) Implementation (compile design into place and route design)
5) Result Analysis (run a test bench and look at ISM simulation results to make corrections if necessary)
6) Debug (close ISM, edit, and try again)
7) Device Programming (download design into device)

Course Policies:
- You are required to come to class and be on time. Assignments are due within 30 minutes of the start of class.
- Late assignments will NOT be accepted without written medical, legal, military, or work justification. Special circumstances will be considered if reported in time. Makeup labs are by appointment only.
- Group discussions and team problem solving is allowed and encouraged to the degree that it can be ensured that all team/group members contribute and understand all required facets of the work at hand.
- Lab assignment documentation (Lab Notebooks) must always be written-up by each student individually and uniquely in his/her own handwriting and in his/her own style.
EE 2169 – “Lab for EE 2369”
Digital Systems Design 1 Lab

- **Pre-Lab**: Pre-Lab assignments are the preparation required for each lab assignment. They should be done in the required lab notebook and must be submitted at the beginning of each lab session. They are part of the overall lab assignment and will be graded as such.

- **Lab Assignments**: Lab assignments should be done in the required lab notebook and must be submitted completed before the next session, and submitted at the beginning of the next lab session. Each student must present a working demonstration of the lab assignment to the instructor before the end of the lab session in order to earn full credit. Getting assistance or assisting other students is allowed, as long as one student does not perform the other’s lab procedure.

- **Final Project**: Implementation of a Digital System design project will be your final lab for the semester.

- **Academic dishonesty will not be tolerated.** If you are suspected of academic dishonesty, you will immediately be referred to the UTEP OSCCR office, without notice or warning.

- Samples of student work will be collected for quality assurance purposes. Please notify the professor, in writing, if there is any confidentiality requirement.

- All printed work must be stapled or glued, with good presentation, for full credit.

**Course Grading:**

- Lab Assignments ......................... 75%
- Final Project ............................... 25%

**Lab Notebook Grading Rubric:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Points</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-Lab</td>
<td>30 pts</td>
</tr>
<tr>
<td>Lab Results</td>
<td>30 pts</td>
</tr>
<tr>
<td>Conclusions</td>
<td>20 pts</td>
</tr>
<tr>
<td>Demonstration</td>
<td>20 pts</td>
</tr>
</tbody>
</table>

**Scale for Letter Grade:**

- 90% – 100% → A
- 80% – 89% → B
- 70% – 79% → C
- 60% – 69% → D
- 0% – 59% → F

**Lab/Lab Notebook Guidance:**

You will be provided with a Lab write-up on a weekly basis. It will have a short reading assignment, Pre-Lab assignment (preparation for the lab), Lab Procedure, and some guiding questions for writing your conclusion.

**Pre-Lab:**

- Calculations (tables, diagrams, K-maps, etc.)
- Justifications – 1 paragraph

**Lab Results:**

- Schematics, HDL, screenshots (pictures), Simulation, etc.
- Justifications – 1 paragraph
- Notes on any problems encountered, and solutions implemented

**Conclusions:**

- Discussion of the objective of the lab (given in the Lab write-up), and what was learned during this lab. Answer questions given in the Lab write-up, which are intended to guide your conclusions.

Some general questions that could be addressed here are:

- What is the relationship between the course lecture and how you implemented this lab?
- Comment on expected and unexpected results during the lab procedure.
EE 2169 – “Lab for EE 2369”
Digital Systems Design I Lab

- How is what you did in this Lab seen in technologies in the real world? Give examples.

Demonstration:
- Demonstrate working software, simulation, or circuit to Teaching Assistant, if applicable.

Academic Dishonesty:
As an entity of The University of Texas at El Paso, the Department of Electrical and Computer Engineering is committed to the development of its students and to the promotion of personal integrity and self-responsibility. The assumption that a student’s work is a fair representation of the student’s ability to perform forms the basis for departmental and institutional quality. All students within the Department are expected to observe appropriate standards of conduct. Acts of scholastic dishonesty such as cheating, plagiarism, collusion, the submission for credit of any work or materials that are attributable in the whole or in part to another person, taking an examination for another person, any act designed to give unfair advantage to a student, or the attempt to commit such acts will not be tolerated. Any case involving academic dishonesty will be referred to the Office of Student Conduct and Conflict Resolution (OSCCR). The Associate Dean of Students will assign a Student Judicial Affairs Coordinator who will investigate the charge and alert the student as to its disposition. Consequences of academic dishonesty may be as severe as dismissal from the University. See the OSCCR homepage at http://sa.utep.edu/osccr/ for more information.

American Disabilities Act:
If you feel you may have a disability that requires accommodations, contact the Center for Accommodations and Support Services (CASS, http://sa.utep.edu/cass) at 747-5148 located in the Union East, Room 106.
# EE 2169

## Digital System Design I Laboratory

Schedule -- Spring 2018

<table>
<thead>
<tr>
<th>Week #</th>
<th>Dates</th>
<th>Lab #</th>
<th>Lab Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Aug. 27 – Aug. 31</td>
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<td>No labs</td>
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<tr>
<td>2</td>
<td>Sep. 4 – Sep. 7</td>
<td>1</td>
<td>Binary Number Systems</td>
</tr>
<tr>
<td>3</td>
<td>Sep. 10 – Sep. 14</td>
<td>2</td>
<td>Switches and LEDs</td>
</tr>
<tr>
<td>4</td>
<td>Sep. 17 – Sep. 21</td>
<td>3</td>
<td>Logic Expressions</td>
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<tr>
<td>5</td>
<td>Sep. 24 – Sep. 28</td>
<td>4</td>
<td>Logic Gates</td>
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<tr>
<td>6</td>
<td>Oct. 1 – Oct. 5</td>
<td>5</td>
<td>Xilinx</td>
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<tr>
<td>7</td>
<td>Oct. 8 – Oct. 12</td>
<td>6</td>
<td>Decimal-Number-to-Braille Encoder Design</td>
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<tr>
<td>8</td>
<td>Oct. 15 – Oct. 19</td>
<td>7</td>
<td>Braille Encoder in Verilog and VHDL</td>
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<tr>
<td>9</td>
<td>Oct. 22 – Oct. 26</td>
<td>8</td>
<td>Full Adder with BCD Display</td>
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<tr>
<td>10</td>
<td>Oct. 29 – Nov. 2</td>
<td>9</td>
<td>Add-Subtract and Shift Register</td>
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<tr>
<td>11</td>
<td>Nov. 5 – Nov. 9</td>
<td>10</td>
<td>FSM: ID display</td>
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<tr>
<td>12</td>
<td>Nov. 12 – Nov. 16</td>
<td>11</td>
<td>ASM: HAWK</td>
</tr>
<tr>
<td>13</td>
<td>Nov. 19 – Nov. 23</td>
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<td>Make-up LAB (short week, Thanksgiving break Nov. 22-23 – UTEP CLOSED)</td>
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<tr>
<td>14</td>
<td>Nov. 26 – Nov. 30</td>
<td>12</td>
<td>ASM: Industrial Parts Transport Controller</td>
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<tr>
<td>15</td>
<td>Dec. 3 – Dec. 7</td>
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<td>Continuation of #12 (short week, Dead Day on Dec.7)</td>
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<tr>
<td>16</td>
<td>Dec. 10 – Dec. 14</td>
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<td>No Labs (Final Exams)</td>
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</table>

* -- denotes tentative topic