

EE 5376 --- Computer Architecture I

Fall 2016

Instructor: Dr. Michael McGarry
Office: Engineering Annex 340
Telephone: 747-6955
Email: mpmcgarry@utep.edu

Text: Computer Organization and Design: The Hardware/Software Interface
by David Patterson and John Hennessy (4th Edition)
Computer Architecture: A Quantitative Approach
by John Hennessy and David Patterson (5th Edition)

Course Description: Techniques used to reduce the two fundamental contributions to clocks per instruction (CPI):

- 1) Average clock cycles for data path execution (CPI_{exec})
 - a. Exploit Instruction Level Parallelism (ILP)
 - i. Pipelined data path
 - ii. Multiple Instruction Issue data path
 - b. Exploit Data Level Parallelism (DLP)
 - i. Vector processors
 - ii. Graphics processing units
- 2) Average clock cycles spent on memory accesses (CPI_{mem})
 - a. Exploit the principle of locality
 - i. Hierarchical memory design

Prerequisite: EE 4379 with a grade of “C” or better. Prerequisite by Topic: (1) assembly language programming (2) computer organization and architecture

Class Hours: Tuesdays and Thursdays 1:30PM to 2:50PM (Classroom Bldg. Rm C204)

Office Hours: Tuesdays 4:30PM to 6PM and Thursdays 12PM to 1:30PM (Eng. A340)

Course Outline:

Weeks 1-2: Computer Performance Analysis Techniques
Week 2: Instruction Set Architecture; MIPS Assembly Language
Weeks 3-4: Processor Architecture: Data Path and Control Path
Weeks 5-6: Pipelining
Week 7: Parallel Structures: Multi-Issue, Multi-Core, Multi-Processor, Cluster
Week 7: Exploiting Parallelism: Job, Thread, Data, and Instruction
Week 8: Midterm; Instruction Level Parallelism (ILP)
Weeks 8-9: Instruction Level Parallelism (ILP)
Weeks 9-10: Exposing ILP through Loop Unrolling
Weeks 11-12: Dynamic Instruction Scheduling
Weeks 12-13: Cache Memory Optimizations
Weeks 14-15: Data Level Parallelism (DLP) (Vector Processors and Graphics Processing Units)

Grading:

Homework/Labs	25%
Survey Article (due 11/17)	25%
Midterm (10/13)	25%
Final (12/8 1PM)	25%

Learning Objectives:

1. Students will understand all of the factors that influence the number of clock cycles it takes to execute an assembly language instruction. These include numbers of clock cycles spent on memory access.
2. Students will understand the different classes of parallelism.
 - a. Job Level Parallelism
 - b. Instruction Level Parallelism
 - c. Thread Level Parallelism
 - d. Data Level Parallelism
3. Students will understand all of the hazards associated with exploiting Instruction Level Parallelism (ILP).
4. Students will understand several techniques to reduce these different factors via Instruction Level Parallelism (ILP) exploitation.
 - a. Pipelining
 - b. Multiple Instruction Issue
 - c. Dynamic Instruction Scheduling
 - d. Loop Unrolling
 - e. Branch Prediction
 - f. Speculative Execution
5. Students will understand several techniques to reduce these different factors via optimization of the hierarchical memory system.
 - a. Critical Word First
 - b. Early Restart
 - c. Way Prediction
6. Students will understand architectures for exploiting data level parallelism
 - a. Vector processors
 - b. Graphics processing units (GPUs)

Academic Dishonesty:

As an entity of The University of Texas at El Paso, the Department of Electrical and Computer Engineering is committed to the development of its students and to the promotion of personal integrity and self responsibility. The assumption that a student's work is a fair representation of the student's ability to perform forms the basis for departmental and institutional quality. All students within the Department are expected to observe appropriate standards of conduct. Acts of scholastic dishonesty such as cheating, plagiarism, collusion, the submission for credit of any work or materials that are attributable in the whole or in part to another person, taking an examination for another person, any act designed to give unfair advantage to a student, or the attempt to commit such acts will not be tolerated. Any case involving academic dishonesty will be referred to the Office of the Dean of Students. The Dean will assign a Student Judicial Affairs Coordinator who will investigate the charge and alert the student as to its disposition. Consequences of academic dishonesty may be as severe as dismissal from the University. See the Office of the Dean of Students' homepage (Office of Student Life) at <http://studentaffairs.utep.edu/dos> for more information.

If you have a disability and need classroom accommodations, please contact The Center for Accommodations and Support Services (CASS) at 747-5148, or by email to cass@utep.edu, or visit their office located in UTEP Union East, Room 106. For additional information, please visit the CASS website at www.sa.utep.edu/cass. *CASS' Staff are the only individuals who can validate and if need be, authorize accommodations for students with disabilities.*