

EE 5376 --- Computer Architecture I

Fall 2015

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Text: Computer Organization and Design: The Hardware/Software Interface
by David Patterson and John Hennessy (4th Edition)
Computer Architecture: A Quantitative Approach
by John Hennessy and David Patterson (5th Edition)

Course Description: Techniques used to reduce the two fundamental contributions to clocks per instruction (CPI):

- 1) Average clock cycles for data path execution (CPI_{exec})
 - a. Exploit Instruction Level Parallelism (ILP)
 - i. Pipelined data path
 - ii. Multiple Instruction Issue data path
 - b. Exploit Data Level Parallelism (DLP)
 - i. Vector processors
 - ii. Graphics processing units
- 2) Average clock cycles spent on memory accesses (CPI_{mem})
 - a. Exploit the principle of locality
 - i. Hierarchical memory design

Prerequisite: EE 4379 with a grade of “C” or better. Prerequisite by Topic: (1) assembly language programming (2) computer organization and architecture

Class Hours: Tuesdays and Thursdays 1:30PM to 2:50PM (CCSB Rm. 1.0204)

Office Hours: Tuesdays 4:30PM to 6PM and Thursdays 12PM to 1:30PM (Eng. A340)

Course Outline:

Weeks 1-2: Computer Performance Analysis Techniques
Week 2: Instruction Set Architecture; MIPS Assembly Language
Weeks 3-4: Processor Architecture: Data Path and Control Path
Weeks 5-6: Pipelining
Week 7: Parallel Structures: Multi-Issue, Multi-Core, Multi-Processor, Cluster
Week 7: Exploiting Parallelism: Job, Thread, Data, and Instruction
Week 8: Midterm; Instruction Level Parallelism (ILP)
Weeks 8-9: Instruction Level Parallelism (ILP)
Weeks 9-10: Exposing ILP through Loop Unrolling
Weeks 11-12: Dynamic Instruction Scheduling
Weeks 12-13: Cache Memory Optimizations
Weeks 14-15: Data Level Parallelism (DLP) (Vector Processors and Graphics Processing Units)

Grading:

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| Homework/Labs | 25% |
| Survey Article (due 11/17) | 25% |
| Midterm (10/15) | 25% |
| Final (12/10 1PM) | 25% |

Learning Objectives:

1. Students will understand all of the factors that influence the number of clock cycles it takes to execute an assembly language instruction. These include numbers of clock cycles spent on memory access.
2. Students will understand the different classes of parallelism.
 - a. Job Level Parallelism
 - b. Instruction Level Parallelism
 - c. Thread Level Parallelism
 - d. Data Level Parallelism
3. Students will understand all of the hazards associated with exploiting Instruction Level Parallelism (ILP).
4. Students will understand several techniques to reduce these different factors via Instruction Level Parallelism (ILP) exploitation.
 - a. Pipelining
 - b. Multiple Instruction Issue
 - c. Dynamic Instruction Scheduling
 - d. Loop Unrolling
 - e. Branch Prediction
 - f. Speculative Execution
5. Students will understand several techniques to reduce these different factors via optimization of the hierarchical memory system.
 - a. Critical Word First
 - b. Early Restart
 - c. Way Prediction
6. Students will understand architectures for exploiting data level parallelism
 - a. Vector processors
 - b. Graphics processing units (GPUs)

Academic Dishonesty:

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