# EE 4379 --- Computer Architecture

*Fall 2016*

**Instructor:** Dr. Michael McGarry
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**Text:** Computer Organization and Design: The Hardware/Software Interface by David Patterson and John Hennessy (5th Edition)

**Optional Reference Texts:**

The C Programming Language by Brian Kernighan and Dennis Ritchie
Verilog HDL by Samir Palnitkar [available as an eBook through UTEP library]

**Course Description:** Binary representation of characters, integers, floating point numbers and assembly language instructions. Integer arithmetic circuit design. Data path and control path design of a non-pipelined and pipelined microprocessor. Multi-processing architectures. Hierarchical memory design.

**Prerequisite:** EE 3376 with a grade of "C" or better. Prerequisite by Topic: (1) combinational and sequential digital design techniques (2) high-level language programming with the C programming language

**Class Hours:** Tuesdays and Thursdays 3:00PM to 4:20PM (CCSB Rm. 1.0202)

**Office Hours:** Tuesdays 4:30PM to 6PM and Thursdays 12PM to 1:30PM (Eng. A340)

**Course Outline:**

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| Weeks 1-2: | Computer Performance Analysis Techniques |
| Week 3: | MIPS Assembly Language |
| Week 4: | Support for Procedures; Instruction Formats |
| Week 5: | Character and Integer Representation; Computer Integer Arithmetic |
| Week 6: | Floating Point Number Representation |
| Week 7: | Verilog HDL |
| Week 8: | Midterm; Processor Architecture: Data Path |
| Week 9: | Processor Architecture: Data Path |
| Week 10: | Processor Architecture: Control Path |
| Week 11: | Pipelining |
| Week 12: | Parallel Structures: Multi-Issue, Multi-Core, Multi-Processor, Cluster |
| Week 12: | Exploiting Parallelism: Job, Thread, Data, and Instruction |
| Weeks 13-14: | Hierarchical Memory Design: Cache Memory |
| Week 15: | Hierarchical Memory Design: Virtual Memory |

**Grading:**

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|---|---|
| Homework/Quiz | 20% |
| Class Participation | 5% |
| Lab 1 (due 9/20) | 5% |
| Lab 2 (due 10/27) | 5% |
| Lab 3 (due 11/3) | 10% |
| Lab 4 (due 11/24) | 15% |
| Midterm (10/13) | 20% |
| Final (12/8 4PM) | 20% |

**Learning Objectives:**

1. Learn methods of analyzing the performance of computer systems
    a. Characterization of program execution time
    b. Characterization of power consumption
    c. Amdahl's law
2. Learn the organization and architecture of computer systems
    a. Hardware/Software Interface (Instruction Set Architecture)
        i. MIPS ISA
    b. Computer Representation of Instructions and Data
        i. Signed/Unsigned Integers
        ii. IEEE 754 Floating Point
        iii. MIPS ISA Instruction Formats
    c. Integer Arithmetic Circuit Design
    d. Basic Microprocessor Design
        i. Data Path (ALU, Register File, etc.)
        ii. Control Path
        iii. Pipelining
    e. Parallel architectures and types of parallelism
        i. Job-level parallelism
        ii. Thread-level parallelism
        iii. Data-level parallelism
        iv. Instruction-level parallelism
        v. Multi-issue, multi-core, multi-processor, cluster
        vi. SISD, SIMD, MIMD
    f. Hierarchical Memory Architectures
        i. Exploiting temporal/spatial locality
        ii. Cache organization
        iii. Cache performance analysis
        iv. Techniques to reduce miss rate
        v. Techniques to reduce miss penalty
        vi. Virtual memory

**Academic Dishonesty:**

As an entity of The University of Texas at El Paso, the Department of Electrical and Computer Engineering is committed to the development of its students and to the promotion of personal integrity and self responsibility. The assumption that a student's work is a fair representation of the student's ability to perform forms the basis for departmental and institutional quality. All students within the Department are expected to observe appropriate standards of conduct. Acts of scholastic dishonesty such as cheating, plagiarism, collusion, the submission for credit of any work or materials that are attributable in the whole or in part to another person, taking an examination for another person, any act designed to give unfair advantage to a student, or the attempt to commit such acts will not be tolerated. Any case involving academic dishonesty will be referred to the Office of the Dean of Students. The Dean will assign a Student Judicial Affairs Coordinator who will investigate the charge and alert the student as to its disposition. Consequences of academic dishonesty may be as severe as dismissal from the University. See the Office of the Dean of Students' homepage (Office of Student Life) at http://studentaffairs.utep.edu/dos for more information.

**If you have a disability and need classroom accommodations, please contact The Center for Accommodations and Support Services (CASS) at 747-5148, or by email to cass@utep.edu, or visit their office located in UTEP Union East, Room 106. For additional information, please visit the CASS website at www.sa.utep.edu/cass.** *CASS' Staff are the only individuals who can validate and if need be, authorize accommodations for students with disabilities.*