EE 2369 – Digital Systems Design I
Schedule

Week #	Lecture #	Date	Topic
1	1	August 27, 2019	Course Information, Syllabus, Introduction to Digital Design
	2	August 29, 2019	Logic Gates, Basic Boolean Operators , Number Systems
2	3	September 3, 2019	Arithmetic and Two's Complement
	4	September 5, 2019	Basic Boolean Algebra, Equations,
3	5	September 10, 2019	Logic Diagrams, Design of Circuits, Timing Diagrams
	6	September 12, 2019	Canonical Equations, Reduced Equations via Boolean Algebra
4	7	September 17, 2019	K-Maps & Reduced Equations
	8	September 19, 2019	Design of Combinational Systems
5	9	September 24, 2019	Quine-McCluskey method of reduction
	10	September 26, 2019	More design considerations
6	11	October 1, 2019	Analysis, reverse engineering
	12	October 3, 2019	Adder design, other gates, implementation guidelines
7	13	October 8, 2019	MSI Devices: MUXes and Decoders, Adders
	14	October 10, 2019	Flip-Flops and timing diagrams
8	15	October 15, 2019	Counter design, Registers
	16	October 17, 2019	Sequential Machines
9	17	October 22, 2019	Mealy and Moore Machines
	18	October 24, 2019	Capturing behavior with FSM
10	19	October 29, 2019	Sequential design considerations
	20	October 31, 2019	State Encodings
11	21	November 5, 2019	Reducing States
	22	November 7, 2019	Algorithmic State Machines methodology
12	23	November 12, 2019	Basic ASM Design
	24	November 14, 2019	ASM Design with MSI
13	25	November 19, 2019	Design Examples
	26	November 21, 2019	ASM Design with LSI
14	27	November 26, 2019	Design Examples
	28	*November 28, 2019*	THANKSGIVING HOLIDAY – University Closed
15	29	December 3, 2019	Controller Clock Frequency
	30	December 5, 2019	Other design considerations (e.g. max. frequency, critical paths, etc.)
16	---	Finals Week	This is an **optional** exam for those that need to replace a partial exam score (see syllabus for details and requirements). You must have taken all 3 partial exams for this option **Comprehensive exam covers all chapters, no sheet of notes allowed.**

This is a **tentative** course schedule. While changes to the schedule are not likely to occur, the instructor has the right to make necessary changes.

Class meets TR 3:00PM - 4:20PM